

### **REMARKS**

The Office Action dated May 17, 2004, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

As a preliminary matter, Applicants appreciate the indication of allowable subject matter in claims 4, 8, 12, 14, 16-20, 24, 28, 32, 34-40, 42, and 44 of the present application.

Claims 1-44 have been cancelled without prejudice. New claims 45-77 have been added. Applicants submit that the new claims herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 45-77 are pending in the present application and are respectfully submitted for consideration.

#### **Claims 1-44 Cancelled**

Claims 8 and 28 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. In addition, claims 1-3, 6-11, 13, 21-23, 26-31, 33, 41, and 43 were rejected under 35 U.S.C. § 102(b) as being anticipated by Whetsel, Jr. (U.S. Patent No. 6,304,987, Whetsel"). Moreover, claims 5, 15 and 25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Whetsel in view of Malladi (U.S. Patent No. 5,598,641, "Malladi").

As mentioned above, claims 1-44 have been cancelled without prejudice. Accordingly, the rejections noted in the outstanding with respect to these claims are now moot.

**New claims 45-77 Recite Patentable Subject Matter**

Claim 45 recites a test circuit that is incorporated in a device. The test circuit is operable to carry out a verification of a first connection node for outputting a signal of the device in a usual operation. The test circuit comprises a test data generating circuit operable to generate test data for carrying out the verification, and a test output buffer connected to the first connection node. The test output buffer is operable to receive test data from the test data generating circuit and to output the test data to the first connection node.

Claim 56 recites a semiconductor integrated circuit device having an output circuit operable to transmit a signal via a first connection node, and a test circuit operable to carry out a connection verification of the first connection node in an usual operation. The test circuit comprises a test data generating circuit operable to generate test data for carrying out the connection verification of the first connection node, and a test output buffer connected to the output circuit. The test output buffer is operable to receive test data from the test data generating circuit and to output the test data to the first connection node.

Claim 71 recites a test circuit operable to carry out a verification of a connection node for outputting a signal in a usual operation. The test circuit comprises a test data generating circuit operable to generate single end test data for carrying out the verification, and a selector circuit, operable to select the single end test data or a signal from an internal circuit based on a test mode signal, the selector circuit being further

operable to convert the selected data or signal to a differential signal, and to output the differential signal.

Claim 72 recites a semiconductor integrated circuit device operable to carry out a verification of a connection node for inputting a signal in a usual operation. The semiconductor integrated circuit comprises a data input buffer operable to receive data input to the connection node, a test input buffer connected to the connection node, operable to receive test data input to the connection node, and a test data processing circuit operable to process the test data.

Hence, the present invention provides, among other features, that the test data generating circuit is connected to an input/output node in parallel, and a test for verifying a connection of nodes can be effectively carried out without reducing operation speed in the usual operation. Further in the present invention, the test circuit is operable to carry out a verification (connection verification) of a (first) connection node (for outputting or inputting a signal) in a usual operation. Therefore, Applicants respectfully submit that claims 45-77 recite subject matter that is neither disclosed nor suggested in any prior art, and therefore are allowable.

In view of the above, Applicants respectfully submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 45-77 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the

Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300 referencing Attorney Docket No. 100021-00074.

Respectfully submitted,



Sam Huang  
Registration No. 48,430

Customer No. 004372  
ARENT FOX, PLLC  
1050 Connecticut Avenue, N.W., Suite 400  
Washington, D.C. 20036-5339  
Tel: (202) 857-6000  
Fax: (202) 638-4810

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Enclosures: Petition for Extension of Time (3 months)